TOSHIBA

Embedded Flash Memory

SCALE TODAY

RAW NAND
MANAGED NAND

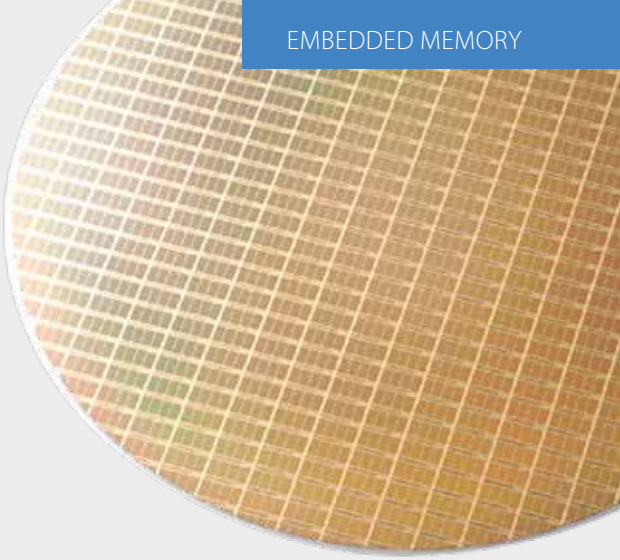
OWN TOMORROW

BiCS FLASH™

INVENTOR OF FLASH MEMORY

Content

Inventor of Flash Memory



Silica wafers are formed from highly pure, nearly defect-free single crystalline material: the starting point for any integrated circuits.

INNOVATION IS OUR TRADITION

In 1984 Toshiba developed a new type of semiconductor memory called flash memory. Later in 1987, NAND flash memory was developed that raised electronic equipment to the next level. The NAND flash market has grown rapidly, with flash memory becoming an internationally standardised memory device. Toshiba, the inventor of flash memory, has thus carved out a path to a new era in which innovations are increased by the opportunities of NAND flash.

SPEED UP DIGITAL PROCESSES

Storing and processing data has always been an important aspect of all digital processes. But in the last years it increased to one of the key technologies for industry 4.0, smart mobility, cloud technology and artificial intelligence, because smart ideas and innovations have to be ready for markets right away – with the highest reliability of storage components.

With our embedded memory solutions, Toshiba is the partner for all smart markets and fast moving industries. Toshiba, the inventor of flash memory in 1984, provides a highly grade of innovation combined with highly reliable security – now and in the future.

PARTNERSHIP IS OUR PASSION

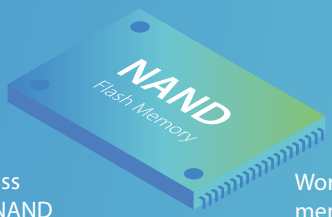
Our success is based on our strong customer focus: Your metrics are our metrics. The result is a broad range of industry-leading flash-based storage solutions. Our products are designed to meet your specific engineering demands.

TOSHIBA EMBEDDED MEMORY – THE KEY TO A SMART FUTURE

Embedded memory connects us with the things that surround and serve us – for more efficiency, comfort and sustainability.

INVENTOR OF FLASH MEMORY

Toshiba's Milestones



INVENTOR OF FLASH MEMORY

1984 World's first flash memory

1987 Invention of the world's first NAND flash memory

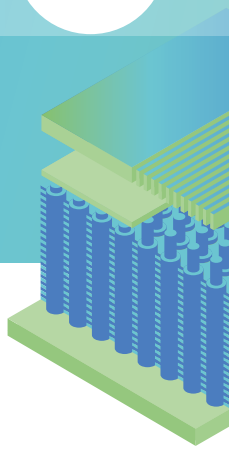
1991 World's first mass production of NAND flash memory

1999 Key milestones for investment and development of Toshiba Flash Technology

2007 World's first 3D flash memory technology announced

2011 World's first 24nm SLC NAND flash memory

2014 World's first 15nm 128 Gbit NAND flash memory



From the invention of flash memory in 1984 to today's break-through BiCS FLASH™ 3D technology (BiCS stands for "Bit Column Stacked"), Toshiba continues to move the industry forward. Whatever the digital future demands, we will keep developing the right solutions for our customers.

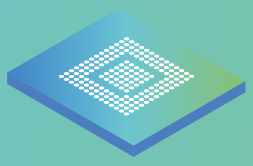
Demanding change

The economy's digital transformation is resulting in a massive increase of data processing, storage and traffic.

48 Layer

64 Layer

96 Layer



World's first 48-layer 3D BiCS FLASH™

Mass production of 96-layer BiCS FLASH™

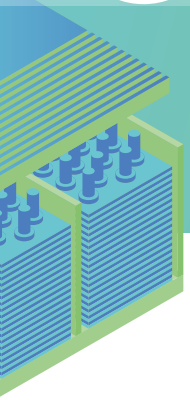
By 2020, 60% of all enterprises will have organisation-wide digital transformation platform strategies

2015 | 2017 | 2018 | 2019 | 2020 | 2021 | 2022

Mass production of 64-layer BiCS FLASH™

By the end of 2019, digital transformation spending is expected to reach $1.7T, up 42% from 2017

By 2021, at least 50% of global GDP will be digitised with growth driven by digitally enhanced offerings, operations and relationships



BiCS FLASH™

165 ZB

1 zettabyte (ZB) = 10^{21} bytes = 1 billion terabytes (TB)

15 ZB

2016 | 2017 | 2018 | 2019 | 2020 | 2021 | 2022

EMBEDDED FLASH MEMORY

SLC NAND
BENAND
Serial NAND
e-MMC
UFS

Toshiba offers a wide range of advanced Flash Memory technology for all kind of applications like consumer electronics, mobile technology and industrial applications such as robotics.

NAND Flash Memory requires an appropriate management, which has to cover tasks like Bad Block Management, Wear Leveling, Garbage Collection and ECC Error Correction. Either these functions are supported by the host system in combination with raw NAND Memory, or it is covered instantly inside a managed NAND by utilizing an integrated memory controller.

The selection between these basic different approaches to control a NAND memory defines the individual host requirements and interface options. For managed NAND there are JEDEC specified Standard-Interfaces supported, enabling the developer to easily design the required memory solution.

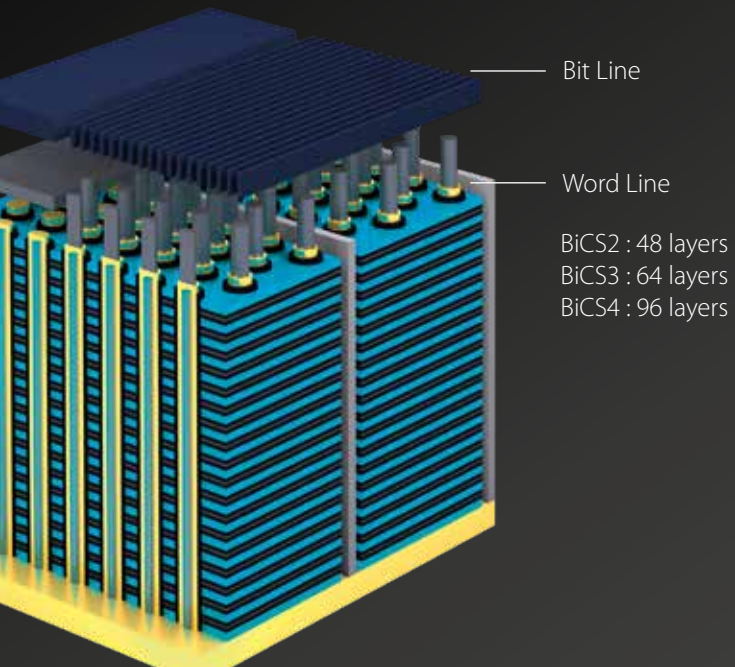
RAW NAND

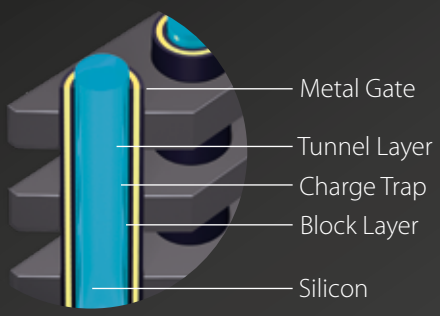
With raw NANDs like SLC NAND, BENAND™ and Serial NAND we provide best in class endurance and data retention for sensitive or frequently used data.

MANAGED NAND

For applications that demand high-speed performance and power efficiency like mobile and automotive uses our managed NANDs e-MMC and UFS support reliable processes at the highest standards. They provide higher capacity and faster programming.

Toshiba 3D NAND - BiCS Flash





Our cutting-edge 3D BiCS FLASH technology with 64- and 96-layer stacking make a powerful memory solutions possible. It gives BiCS FLASH far higher die area density compared to 2D NAND. BiCS FLASH reduces the chip size by optimizing both circuit technology and the manufacturing process.

BiCS FLASH™

SLC NAND

Reliability and Performance

Toshiba's advanced Flash Memory technology offers SLC NAND providing best in class endurance and data retention for sensitive or frequently used data in a system. For long lasting products or systems working with extremely high data throughput between the host and the memory, Toshiba SLC is the optimal solution.

SPECIFICATIONS

FEATURES	SLC NAND
Density	1 Gbit – 128 Gbit
Technology	24nm
ECC (Error Correction Code)	Required on Host Side
Temperature	-40 °C to 85 °C 0 °C to 70 °C
Package	TSOP and BGA

CAPACITIES:

1 Gbit · 2 Gbit · 4 Gbit · 8 Gbit · 16 Gbit · 32 Gbit · 64 Gbit · 128 Gbit

KEY FEATURES:

- 1 Gbit – 128 Gbit
- Extended temperature range
- TSOP and BGA package

ADVANTAGES

- Broad line up to cover customers' demands for different densities
- Leading-edge 24nm technology for cost optimisation
- Long data retention or extreme write/erase performance
- Small package variation available to reduce board space by 48 % (up to 8 Gbit)
- Produced in the world's largest, leading edge technology flash factory

APPLICATIONS:

- Industrial Applications
- Consumer Electronics
- Multimedia Applications
- Smart Metering & Intelligent Lighting
- Smart Applications

INVENTOR OF FLASH MEMORY

BENAND™

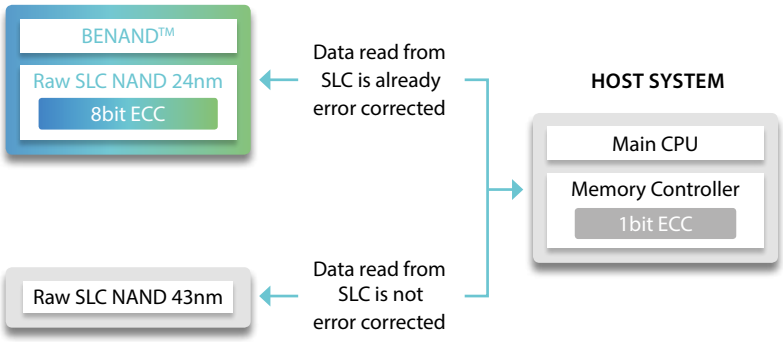
Reliability and Performance

Toshiba's BENAND™ removes the burden of Error Correction Code (ECC) from the host processor by offering ECC embedded in the hardware while keeping the same specification, high reliability and performance as a raw SLC.

SPECIFICATIONS

FEATURES	BENAND™ (SLC+ECC)
Density	1 Gbit – 8 Gbit
Technology	24nm
ECC (Error Correction Code)	Embedded on Memory Chip
Temperature	-40 °C to 85 °C 0 °C to 70 °C
Package	TSOP and BGA

BENAND™ – SLC WITH EMBEDDED ECC FOR BOM REDUCTION AND SYSTEM FLEXIBILITY



CAPACITIES:

1 Gbit | 2 Gbit | 4 Gbit | 8 Gbit

KEY FEATURES:

- 1 Gbit – 8 Gbit
- Same reliability and performance as raw SLC
- Same Hardware interface and package as raw SLC

ADVANTAGES:

- Broad line-up to cover customers' demands for different densities
- Leading edge 24nm technology for cost optimisation
- Long data retention or extreme write/erase performance
- Small package variation available to reduce board space by 48 % (up to 8 Gbit)
- With BENAND™ no ECC operation is required on the host side
- Produced in the world's largest, leading edge technology flash factory

APPLICATIONS:

- Industrial Applications
- Consumer Electronics
- Multimedia Applications
- Smart Metering & Intelligent Lighting
- Smart Applications

SERIAL NAND

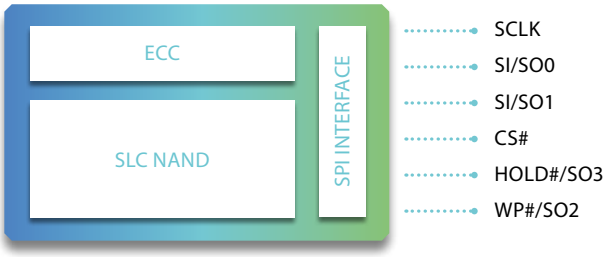
SLC NAND with SPI Interface

Toshiba's new line-up of 24nm-based Serial NAND flash memory products is compatible with the widely used Serial Peripheral Interface (SPI), giving users access to SLC NAND flash memory with a low pin count, small package and large capacity.

SPECIFICATIONS

FEATURES	SERIAL NAND
Density	1 Gbit – 8 Gbit
Technology	24nm SLC
Interface	Quad-SPI (Serial Peripheral Interface)
ECC (Error Correction Code)	Embedded on Memory Chip
Temperature	-40 °C to 85 °C
Package	8 pin WSON

SERIAL NAND – SLC WITH ECC AND SPI INTERFACE



CAPACITIES:

1 Gbit · 2 Gbit · 4 Gbit · 8 Gbit

KEY FEATURES:

- 1 Gbit – 8 Gbit
- Compatible with SPI Standard
- Extended temperature range
- WSON package
- On-chip hardware ECC which can be turned off/on
- Unique Bit flip report function
- Data protection feature
- High speed sequential read mode
- SPI (x1, x2, x4) Mode 0, Mode 3

ADVANTAGES:

- Broad line-up to cover customers' demands for different densities
- Leading-edge 24nm technology for cost optimization
- Long data retention or extreme write/erase performance
- Small package for reduced board space
- Standardised high-speed serial interface (SPI)
- No ECC operation is required on the host side
- Produced in the world's largest, leading edge technology flash factory

APPLICATIONS:

- Industrial Applications
- Consumer Electronics
- Multimedia Applications
- Smart Metering & Intelligent Lighting
- Smart Applications

INVENTOR OF FLASH MEMORY

e-MMC

Cost Effective Mass Storage

e-MMC is a family of advanced and highly efficient NAND flash memory with an integrated controller and enhanced memory management. Based on an interface standardised by JEDEC, Toshiba's e-MMC offers the optimal solution for applications where higher data volumes need to be stored in a cost-efficient way. It is fully compliant with the Multimedia Card Association (MMCA) high-speed memory interface standard.

SPECIFICATIONS

FEATURES	e-MMC	EXTENDED TEMP. e-MMC
Density	4 GB – 128 GB	8 GB – 64 GB
Technology	15nm FG / BiCS 3D NAND	15nm
JEDEC Version	5.0 / 5.1	5.1
Temperature	-25 °C to 85 °C	-40 °C to 105 °C
Package	FBGA	

e-MMC – DESIGN GUIDELINE & DESIGN CHECK SHEET

To support your e-MMC design, Toshiba offers a design guideline and a design check sheet. The design guideline highlights some of the key topics to be considered when selecting and utilising a Toshiba e-MMC. The design check sheet can be used by the developer to share more detailed information about the individual usage scenario with Toshiba. Both files are available at your local Toshiba representative or qualified distributor.

e-MMC – ENHANCED USER DATA AREA

Toshiba e-MMC products support the JEDEC compliant "Enhanced User Data Area", also called "pseudo-SLC". For applications requiring the memory to perform with higher write/erase cycles than MLC NAND can offer, the e-MMC provides the option to build a partition which offers "pseudo-SLC" performance.

CAPACITIES:

4 GB · 8 GB · 16 GB · 32 GB · 64 GB · 128 GB

KEY FEATURES:

- 4 GB – 128 GB
- 15nm FG / BiCS 3D NAND
- MLC technology
- Conforms to the latest JEDEC Version 5.0 and 5.1
- Integrated memory management:
  - Error correction code
  - Bad block management
  - Wear-levelling
  - Garbage collection
- Standard and extended temperature range of up to 105 °C
- FBGA package

ADVANTAGES

- Higher Interface speed HS400 in accordance with JEDEC 5.x
- Managed memory
- Package, interface, features, commands, etc. are standard
- Utilises high quality Toshiba MLC NAND flash memory in combination with a Toshiba origin developed controller
- Produced in the world's largest, state-of-the-art factory for flash technology

APPLICATIONS:

- Industrial Applications
- Consumer Electronics
- Multimedia Applications
- Smart Metering & Intelligent Lighting
- Smart Applications

INVENTOR OF FLASH MEMORY

BiCS FLASH™

UFS

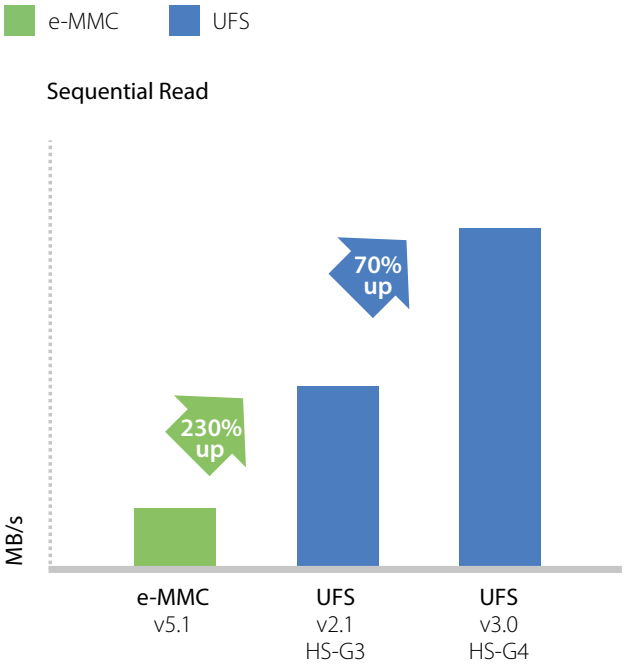
High Performance Mass Storage

Toshiba's flash memories with an integrated controller provide error correction, wear levelling, bad-block management, etc. They have an interface compliant with JEDEC/UFS Version 2.1 / 3.0, eliminating the need for users to perform NAND-specific control. The new full-duplex serial high-speed interface offers superior performance.

SPECIFICATIONS

FEATURES	UFS – UNIVERSAL FLASH STORAGE
Density	32 GB – 512 GB
Technology	BiCS 3D NAND
JEDEC Version	2.1 / 3.0
Temperature	-25 °C to 85 °C
Package	153 ball FBGA (11.5 x 13 mm²)

COMPARING THE PERFORMANCE:



CAPACITIES:

32 GB | 64 GB | 128 GB | 256 GB | 512 GB

KEY FEATURES:

- 32 GB – 512 GB
- BiCS Flash™ Technology (3D NAND)
- Conforms to JEDEC Version 2.1 / 3.0
- Integrated memory management:
  - Error correction code
  - Bad block management
  - Wear-levelling
  - Garbage collection
- Standard temperature range
- 153 ball BGA FBGA package
- High Speed Serial interface

ADVANTAGES

- High speeds up to 1160 MB/sec / 2320 MB/sec
- Managed memory
- Package, interface, features, commands, etc. are standard
- Utilises high quality Toshiba BiCS Flash™ memory in combination with a Toshiba origin developed controller
- Produced in the world's largest, leading edge technology flash factory

APPLICATIONS:

- Consumer Electronics
- Multimedia Applications
- Industrial Applications
- Smart Applications

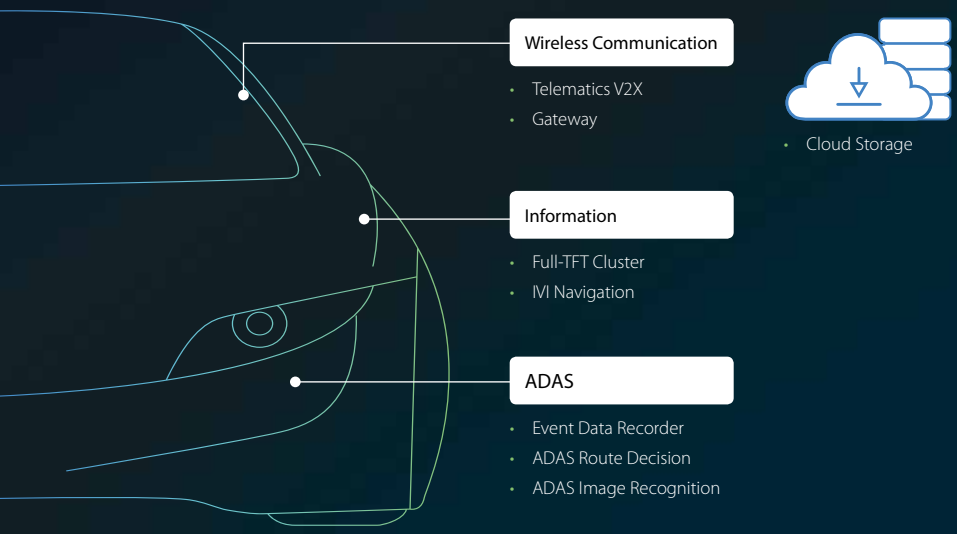
INVENTOR OF FLASH MEMORY

BiCS FLASH™

e-MMC / UFS Automotive

e-MMC / UFS for automotive demands

E-mobility, autonomous driving, higher demands on safety and sustainability – automotive industries are once more leading in innovation and technology. For these smart and connected vehicles, reliable storage solutions are mandatory. Toshiba provides one of the key technologies for wireless communication, information systems and Advanced Driver Assistance Systems (ADAS).



KEY FEATURES:

- AEC-Q100 qualified
- Compliant with IATF16949
- Temperature range: Automotive Grade 2 (-40 °C ~ +105 °C)
- Conforms to JEDEC standard
- Highly reliable 15nm MLC technology
- Integrated memory management:
  - Error correction code
  - Bad block management
  - Wear-levelling
  - Garbage collection
- Automotive specific functions

AUTOMOTIVE APPLICATIONS:

- In-Vehicle Infotainment (IVI)
- Advanced driver-assistance systems (ADAS)
- Cluster
- Telematics
- Gateway
- etc.

e-MMC – AEC-Q100 GRADE 2

DENSITY	PART NUMBER	JEDEC STANDARD	MAX. SPEED (MB/s)	POWER SUPPLY VOLTAGE		TEMPERATURE	PACKAGE
				Vcc (V)	VccQ (V)		
8 GB	THGBMJG6C1LBAB7	JEDEC 5.1	400	2.7 – 3.6	1.7 – 1.95 2.7 – 3.6	-40 °C to 105 °C	FBGA153
16 GB	THGBMJG7C2LBAB8						
32 GB	THGBMJG8C4LBAB8						
64 GB	THGBMJG9C8LBAB8						

UFS – AEC-Q100 GRADE 2

DENSITY	PART NUMBER	JEDEC STANDARD	MAX. SPEED (MB/s)	POWER SUPPLY VOLTAGE		TEMPERATURE	PACKAGE
				Vcc (V)	VccQ (V)		
16 GB	THGAF9G7L1LBAB7	JEDEC 2.1	1160	2.7 – 3.6	1.7 – 1.95	-40 °C to 105 °C	FBGA153
32 GB	THGAF9G8L2LBAB7						
64 GB	THGAF9G9L4LBAB8						
128 GB	THGAF9T0L8LBAB8						

INVENTOR OF FLASH MEMORY

Design Guideline

MANAGED NAND
e-MMC

TEMPERATURE RANGE

- The standard operational temperature is -25 °C ~+85 °C
- If extended temperature range is required, Toshiba offer a product group with -40 °C ~+105 °C
- Important is to check at what typical temperature the e-MMC will actually be used in average
- The given range of temperature is just showing the operational area for the e-MMC, but does not indicate how long the expected data retention will be available if used under very high temperature condition.
- If the e-MMC will be operated constantly at significant higher temperature than 40 °C, it is strongly recommended to discuss with Toshiba about the individual use case, as this could lead to unexpected short data retention. Please utilize the Design Check Sheet to communicate this with Toshiba.
- Optional way to make data more robust against higher temperature is to use the "Enhanced User Data Area" or so called pseudo-SLC. Note that this will halve the available density.

SPEED PERFORMANCE

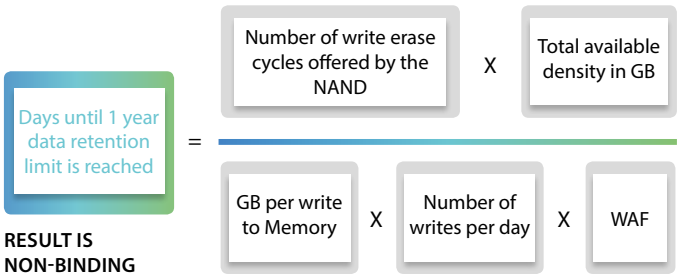
- There is a relation between the density and the write / read performance Please check the individual data sheet of the product
- If the application requires a faster data throughput than the standard e-MMC can offer, there are options like this:
  A) If mainly read speed is targeted to be improved, the change from HS200 to HS400 interface is a possible solution. Note: HS400 is available from JEDEC 5.0 onwards and require an additional pin for the interface.
  B) If mainly the write speed is targeted to be improved, the change to the "Enhanced User Data Area" or so called "pseudo-SLC" would be very efficient. Note that this will halve the available density.

JEDEC BACKWARD COMPATIBILITY

- JEDEC Association is defining the standard of e-MMC, e.g. pin-layout, register naming and utilization, power supply, controller features
- For each update on these standards a new number is given e.g. 4.5, 5.0 and 5.1. A new number shows that this generation of e-MMC supports features of the generation before plus new enhanced features
- A design made for an older Version of e-MMC (e.g. 4.5) can use the latest generation e-MMC (e.g. 5.1) as well. Just the additional new features or interface options of the new generation are not available, but all features of the old generation are still implemented in the new generation
- NOTE: Possible obstacle can be the driver of the MMC interface on the host. This may initially ask for the JEDEC version of the e-MMC and may stop in case the return value is an unknown number to this driver. Here the driver needs to be updated to avoid this issue.

DATA RETENTION & WRITE / ERASE CYCLE

- Main influence on the data retention: Number of write/erase cycles during life time and the operation temperature
- The MLC based NAND inside an e-MMC offers ~ 3K write erase cycles at 40 °C.
- If this is sufficient for the expected life time of a product using the e-MMC strongly depends on the individual usage scenario.
- For e-MMC the WAF (Write Amplification Factor) has to be considered in the calculation of the expected lifetime of the memory
- Formula:



RESULT IS NON-BINDING

- If based on this tentative calculation the lifetime of the e-MMC under a given usage scenario is not sufficient in relation to the expected life time of the product there are options to improve the situation
  A) Use the "Enhanced User Data Area" or so called pseudo-SLC. This will increase the available write erase cycles from ~3K to up to ~max.20K (@40 °C). Note: This will halve the available density.
  B) Increase the density of the e-MMC. The more density is available, the more area for wear leveling is usable for the memory controller, so the w/e stress for the individual cells is reduced.

DATA LOADING BEFORE SOLDERING

- The solder process is stressing the NAND cell extremely due to the high temperature of ~260 °C
- There is a potential negative influence on the data retention or danger for data loss.
- Toshiba e-MMC offers a special Firmware feature, to avoid data loss during the soldering process. Note: There are limitation in the maximum size of data which can be handled by this feature. Please check details with Toshiba via the Design Check Sheet.

Product list

SLC NAND

DENSITY	PART NUMBER	TECHN.	PAGE SIZE	VCC	ECC	TEMPERATURE	PACKAGE
1 Gbit	TC58NVG0S3HTA00	24nm	(2048+128) x 8 bit	3.3V	8bit/512B	0 °C to 70 °C	48TSOP 12 x 20
	TC58NYG0S3HBAI4		(2048+128) x 8 bit	1.8V		-40 °C to 85 °C	63BGA 9 x 11
	TC58NVG0S3HTAI0		(2048+128) x 8 bit	3.3V		-40 °C to 85 °C	48TSOP 12 x 20
	TC58NVG0S3HBAI4		(2048+128) x 8 bit	3.3V		-40 °C to 85 °C	63BGA 9 x 11
	TC58NYG0S3HBAI6		(2048+128) x 8 bit	1.8V		-40 °C to 85 °C	67BGA 6.5 x 8
	TC58NVG0S3HBAI6		(2048+128) x 8 bit	3.3V		-40 °C to 85 °C	67BGA 6.5 x 8
2 Gbit	TC58NVG1S3HTA00	24nm	(2048+128) x 8 bit	3.3V	8bit/512B	0 °C to 70 °C	48TSOP 12 x 20
	TC58NYG1S3HBAI4		(2048+128) x 8 bit	1.8V		-40 °C to 85 °C	63BGA 9 x 11
	TC58NVG1S3HTAI0		(2048+128) x 8 bit	3.3V		-40 °C to 85 °C	48TSOP 12 x 20
	TC58NVG1S3HBAI4		(2048+128) x 8 bit	3.3V		-40 °C to 85 °C	63BGA 9 x 11
	TC58NYG1S3HBAI6		(2048+128) x 8 bit	1.8V		-40 °C to 85 °C	67BGA 6.5 x 8
	TC58NVG1S3HBAI6		(2048+128) x 8 bit	3.3V		-40 °C to 85 °C	67BGA 6.5 x 8
4 Gbit	TH58NVG2S3HTA00	24nm	(2048+128) x 8 bit	3.3V	8bit/512B	0 °C to 70 °C	48TSOP 12 x 20
	TC58NVG2S0HTA00		(4096+256) x 8 bit	3.3V		0 °C to 70 °C	48TSOP 12 x 20
	TC58NVG2S0HTAI0		(4096+256) x 8 bit	3.3V		-40 °C to 85 °C	48TSOP 12 x 20
	TH58NVG2S3HTAI0		(2048+128) x 8 bit	3.3V		-40 °C to 85 °C	48TSOP 12 x 20
	TH58NVG2S3HBAI4		(2048+128) x 8 bit	3.3V		-40 °C to 85 °C	63BGA 9 x 11
	TH58NYG2S3HBAI4		(2048+128) x 8 bit	1.8V		-40 °C to 85 °C	63BGA 9 x 11
	TC58NVG2S0HBAI4		(4096+256) x 8 bit	3.3V		-40 °C to 85 °C	63BGA 9 x 11
	TC58NYG2S0HBAI4		(4096+256) x 8 bit	1.8V		-40 °C to 85 °C	63BGA 9 x 11
	TC58NVG2S0HBAI6		(4096+256) x 8 bit	3.3V		-40 °C to 85 °C	67BGA 6.5 x 8
	TC58NYG2S0HBAI6		(4096+256) x 8 bit	1.8V		-40 °C to 85 °C	67BGA 6.5 x 8
8 Gbit	TH58NVG3S0HTA00	24nm	(4096+256) x 8 bit	3.3V	8bit/512B	0 °C to 70 °C	48TSOP 12 x 20
	TH58NVG3S0HBAI4		(4096+256) x 8 bit	3.3V		-40 °C to 85 °C	63BGA 9 x 11
	TH58NYG3S0HBAI4		(4096+256) x 8 bit	1.8V		-40 °C to 85 °C	63BGA 9 x 11
	TH58NVG3S0HTAI0		(4096+256) x 8 bit	3.3V		-40 °C to 85 °C	48TSOP 12 x 20
	TH58NVG3S0HBAI6		(4096+256) x 8 bit	3.3V		-40 °C to 85 °C	67BGA 6.5 x 8
	TH58NYG3S0HBAI6		(4096+256) x 8 bit	1.8V		-40 °C to 85 °C	67BGA 6.5 x 8
16 Gbit	TH58NVG4S0HTA20	24nm	(4096+256) x 8 bit	3.3V	8bit/512B	0 °C to 70 °C	48TSOP 12 x 20
	TH58NVG4S0HTAK0		(4096+256) x 8 bit	3.3V		-40 °C to 85 °C	48TSOP 12 x 20
32 Gbit	TC58NVG5H2HTA00	24nm	(8192+1024) x 8 bit	3.3V	24bit/1024B	0 °C to 70 °C	48TSOP 12 x 20
	TC58NVG5H2HTAI0		(8192+1024) x 8 bit	3.3V		-40 °C to 85 °C	48TSOP 12 x 20
64 Gbit	TH58NVG6H2HTAK0	24nm	(8192+1024) x 8 bit	3.3V	24bit/1024B	-40 °C to 85 °C	48TSOP 12 x 20
128 Gbit	TH58NVG7H2HTA20	24nm	(8192+1024) x 8 bit	3.3V	24bit/1024B	0 °C to 70 °C	48TSOP 12 x 20

SERIAL NAND

DENSITY	PART NUMBER	PAGE SIZE	VCC	TEMPERATURE	PACKAGE
1 Gbit	TC58CVG0S3HRAIG	(2048+64) x 8 bit	3.3V	-40 °C to 85 °C	8WSON 6x8
	TC58CYG0S3HRAIG		1.8V		
2 Gbit	TC58CVG1S3HRAIG	(2048+64) x 8 bit	3.3V	-40 °C to 85 °C	8WSON 6x8
	TC58CYG1S3HRAIG		1.8V		
4 Gbit	TC58CVG2S0HRAIG	(4096+128) x 8 bit	3.3V	-40 °C to 85 °C	8WSON 6x8
	TC58CYG2S0HRAIG		1.8V		
8 Gbit	TBD	(4096+128) x 8 bit	3.3V	-40 °C to 85 °C	8WSON 6x8
	TBD		1.8V		

Product list

BENAND™

DENSITY	PART NUMBER	TECHN.	PAGE SIZE	VCC	ECC	TEMPERATURE	PACKAGE
1 Gbit	TC58BVG0S3HTA00	24nm	(2048+64) x 8 bit	3.3V	internal ECC	0 °C to 70 °C	48TSOP 12 x 20
	TC58BYG0S3HBAI4		(2048+64) x 8 bit	1.8V		-40 °C to 85 °C	63BGA 9 x 11
	TC58BVG0S3HTAI0		(2048+64) x 8 bit	3.3V		-40 °C to 85 °C	48TSOP 12 x 20
	TC58BVG0S3HBAI4		(2048+64) x 8 bit	3.3V		-40 °C to 85 °C	63BGA 9 x 11
	TC58BYG0S3HBAI6		(2048+64) x 8 bit	1.8V		-40 °C to 85 °C	67BGA 6.5 x 8
	TC58BVG0S3HBAI6		(2048+64) x 8 bit	3.3V		-40 °C to 85 °C	67BGA 6.5 x 8
2 Gbit	TC58BVG1S3HTA00	24nm	(2048+64) x 8 bit	3.3V	internal ECC	0 °C to 70 °C	48TSOP 12 x 20
	TC58BYG1S3HBAI4		(2048+64) x 8 bit	1.8V		-40 °C to 85 °C	63BGA 9 x 11
	TC58BVG1S3HTAI0		(2048+64) x 8 bit	3.3V		-40 °C to 85 °C	48TSOP 12 x 20
	TC58BVG1S3HBAI4		(2048+64) x 8 bit	3.3V		-40 °C to 85 °C	63BGA 9 x 11
	TC58BYG1S3HBAI6		(2048+64) x 8 bit	1.8V		-40 °C to 85 °C	67BGA 6.5 x 8
	TC58BVG1S3HBAI6		(2048+64) x 8 bit	3.3V		-40 °C to 85 °C	67BGA 6.5 x 8
4 Gbit	TH58BVG2S3HTA00	24nm	(2048+64) x 8 bit	3.3V	internal ECC	0 °C to 70 °C	48TSOP 12 x 20
	TC58BVG2S0HTA00		(4096+128) x 8 bit	3.3V		0 °C to 70 °C	48TSOP 12 x 20
	TC58BVG2S0HTAI0		(4096+128) x 8 bit	3.3V		-40 °C to 85 °C	48TSOP 12 x 20
	TH58BVG2S3HTAI0		(2048+64) x 8 bit	3.3V		-40 °C to 85 °C	48TSOP 12 x 20
	TH58BVG2S3HBAI4		(2048+64) x 8 bit	3.3V		-40 °C to 85 °C	63BGA 9 x 11
	TH58BYG2S3HBAI4		(2048+64) x 8 bit	1.8V		-40 °C to 85 °C	63BGA 9 x 11
	TC58BVG2S0HBAI4		(4096+128) x 8 bit	3.3V		-40 °C to 85 °C	63BGA 9 x 11
	TC58BYG2S0HBAI4		(4096+128) x 8 bit	1.8V		-40 °C to 85 °C	63BGA 9 x 11
	TC58BVG2S0HBAI6		(4096+128) x 8 bit	3.3V		-40 °C to 85 °C	67BGA 6.5 x 8
	TC58BYG2S0HBAI6		(4096+128) x 8 bit	1.8V		-40 °C to 85 °C	67BGA 6.5 x 8
	TH58BYG2S3HBAI6		(2048+64) x 8 bit	1.8V		-40 °C to 85 °C	67BGA 6.5 x 8
8 Gbit	TH58BVG3S0HTA00	24nm	(4096+128) x 8 bit	3.3V	internal ECC	0 °C to 70 °C	48TSOP 12 x 20
	TH58BYG3S0HBAI4		(4096+128) x 8 bit	1.8V		-40 °C to 85 °C	63BGA 9 x 11
	TH58BVG3S0HTAI0		(4096+128) x 8 bit	3.3V		-40 °C to 85 °C	48TSOP 12 x 20
	TH58BVG3S0HBAI4		(4096+128) x 8 bit	3.3V		-40 °C to 85 °C	63BGA 9 x 11
	TH58BVG3S0HBAI6		(4096+128) x 8 bit	3.3V		-40 °C to 85 °C	67BGA 6.5 x 8
	TH58BYG3S0HBAI6		(4096+128) x 8 bit	1.8V		-40 °C to 85 °C	67BGA 6.5 x 8

e-MMC

DENSITY	PART NUMBER	TECHN.	JEDEC STANDARD	TEMPERATURE	PACKAGE
4 GB	THGBMNG5D1LBAIT	2D 15nm	JEDEC 5.0	-25 °C to 85 °C	153FBGA 11 x 10
	THGBMNG5D1BAIL			-25 °C to 85 °C	153FBGA 11.5 x 13
8 GB	THGBMJG6C1LBAIL	2D 15nm	JEDEC 5.1	-25 °C to 85 °C	153FBGA 11.5 x 13
	THGBMJG6C1LBAU7			-40 °C to 105 °C	153FBGA 11.5 x 13
16 GB	THGBMJG7C1LBAIL	2D 15nm	JEDEC 5.1	-25 °C to 85 °C	153FBGA 11.5 x 13
	THGBMJG7C2LBAU8			-40 °C to 105 °C	153FBGA 11.5 x 13
	THGAMRG7T13BAIL	3D BiCS3		-25 °C to 85 °C	153FBGA 11.5 x 13
32 GB	THGBMJG8C2LBAIL	2D 15nm	JEDEC 5.1	-25 °C to 85 °C	153FBGA 11.5 x 13
	THGBMJG8C4LBAU8			-40 °C to 105 °C	153FBGA 11.5 x 13
	THGAMRG8T13BAIL	BiCS 3D NAND		-25 °C to 85 °C	153FBGA 11.5 x 13
64 GB	THGBMJG9C8LBAU8	2D 15nm	JEDEC 5.1	-40 °C to 105 °C	153FBGA 11.5 x 13
	THGAMRG9T23BAIL	BiCS 3D NAND		-25 °C to 85 °C	153FBGA 11.5 x 13
128 GB	THGAMRT0T43BAIR	BiCS 3D NAND	JEDEC 5.1	-25 °C to 85 °C	153FBGA 11.5 x 13

UFS

DENSITY	PART NUMBER	TECHNOLOGY	JEDEC STANDARD	TEMPERATURE	PACKAGE
32 GB	THGAF4G8N2LBAIR	BiCS 3D NAND	JEDEC 2.1	-25 °C to 85 °C	153FBGA 11.5 x 13
64 GB	THGAF8G9T43BAIR	BiCS 3D NAND	JEDEC 2.1	-25 °C to 85 °C	153FBGA 11.5 x 13
128 GB	THGBMJG9C8LBAU8	BiCS 3D NAND	JEDEC 2.1	-25 °C to 85 °C	153FBGA 11.5 x 13
	THGAMRG9T23BAIL		JEDEC 3.0		
256 GB	THGAF8T1T83BAIR	BiCS 3D NAND	JEDEC 2.1	-25 °C to 85 °C	153FBGA 11.5 x 13
	THGJFCT1T44BAIL		JEDEC 3.0		
512 GB	THGJFCT2T84BAIC	BiCS 3D NAND	JEDEC 3.0	-25 °C to 85 °C	153FBGA 11.5 x 13

TOSHIBA

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Further information
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Mouser Electronics

Authorized Distributor

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